4. (Amended) The device of claim 1 wherein said resinous layer comprises a material selected from the group consisting of methyl ester of acrylic acid, ethyl ester of acrylic acid, butyl ester of acrylic acid, and 2-ethylhexyl ester of acrylic acid.

5. (Amended) A semiconductor device comprising:

a resinous substrate having an uneven surface;

a resinous layer provided on said uneven surface of said resinous substrate and having a planarized surface; and

a thin-film transistor provided on said planarized surface of said resinous layer;

an interlayer dielectric layer comprising a resinous material provided over said thin-film transistor; and

[an indium tin oxide layer] at least one pixel electrode provided on said interlayer dielectric layer,

wherein said thin-film transistor comprises:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween, and

wherein said semiconductor layer comprises silicon and is obtained by crystallizing amorphous silicon.

7. (Amended) The device of claim 5 wherein said resinous layer comprises a material selected from the group consisting of methyl ester of acrylic acid, ethyl ester of acrylic acid, butyl ester of acrylic acid, and 2-ethylhexyl ester of acrylic acid.

11. (Amended) A semiconductor device comprising:

a resinous substrate having an uneven surface;

a resinous layer provided on said uneven surface of said resinous substrate and

having a planarized surface; and

a transistor provided on said planarized surface of said resinous layer, said transistor comprising:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region;

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween,

wherein said semiconductor layer comprises microcrystalline silicon.

15. (Amended) The device of claim 11 wherein said resinous layer comprises a material selected from the group consisting of methyl ester of acrylic acid, ethyl ester of acrylic acid, butyl ester of acrylic acid, and 2-ethylhexyl ester of acrylic acid.

16. (Amended) The device of claim 12 wherein said resinous layer comprises a material selected from the group consisting of methyl ester of acrylic acid, ethyl ester of acrylic acid, butyl ester of acrylic acid, and 2-ethylhexyl ester of acrylic acid.

Please add the following new claims:

--17. The device of claim 5 wherein said pixel electrode comprises an indium tin oxide.

18. A semiconductor device comprising:

a resinous substrate having an uneven surface;

a resinous layer provided on said uneven surface of said resinous substrate and having a planarized surface; and

a thin film transistor provided on said planarized surface of said resinous layer, and said thin film transistor comprising:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region;

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween,

wherein said channel formation region comprises amorphous silicon.

19. The device of claim 18 wherein said thin film transistor is an inverted-staggered thin-film transistor.

20. The device of claim 18 wherein said substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

21. The device of claim 18 wherein said resinous layer comprises a material selected from the group consisting of methyl ester of acrylic acid, ethyl ester of acrylic acid, butyl ester of acrylic acid and 2-ethylhexyl ester of acrylic acid

22. The device of claim 18 wherein said interlayer dielectric layer comprises polyimide.

23. A semiconductor device comprising:

a resinous substrate having an uneven surface;

a resinous layer provided on said uneven surface of said resinous substrate and having a planarized surface; and

a thin film transistor provided on said planarized surface of said resinous layer;

an interlayer dielectric layer comprising a resinous material provided over said thin-film transistor;

at least one pixel electrode provided on said interlayer dielectric layer,

wherein said thin film transistor comprising:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region;

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween,

wherein said semiconductor layer comprises amorphous silicon.

24. The device of claim 23 wherein said thin film transistor is an inverted-staggered thin-film transistor.

25. The device of claim 23 wherein said substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

26. The device of claim 23 wherein said resinous layer comprises a material selected from the group consisting of methyl ester of acrylic acid, ethyl ester of acrylic acid, butyl ester of acrylic acid and 2-ethylhexyl ester of acrylic acid.

27. The device of claim 23 wherein said interlayer dielectric layer comprises polyimide.

28. A semiconductor device comprising:

a resinous substrate having an uneven surface;

a resinous layer provided on said uneven surface of said resinous substrate and having a planarized surface; and

a thin-film transistor provided on said planarized surface of said resinous layer,

wherein said thin-film transistor comprises:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween, and

wherein said channel formation region comprises microcrystalline silicon.

29. The device of claim 28 wherein said thin film transistor is an inverted-staggered thin-film transistor.

30. The device of claim 28 wherein said substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

31. The device of claim 28 wherein said resinous layer comprises a material selected from the group consisting of methyl ester of acrylic acid, ethyl ester of acrylic acid, butyl ester of acrylic acid and 2-ethylhexyl ester of acrylic acid

32. The device of claim 28 wherein said pixel electrode comprises an indium tin oxide.

33. A semiconductor device comprising:

a resinous substrate having an uneven surface;

a resinous layer provided on said uneven surface of said resinous substrate and having a planarized surface; and

a thin-film transistor provided on said planarized surface of said resinous layer;

an interlayer dielectric layer comprising a resinous material provided over said thin-film transistor; and

at least one pixel electrode provided on said interlayer dielectric layer,

wherein said thin-film transistor comprises:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween, and

wherein said semiconductor layer comprises microcrystalline silicon.

34. The device of claim 33 wherein said thin film transistor is an inverted-staggered thin-film transistor.

35. The device of claim 33 wherein said substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

36. The device of claim 33 wherein said resinous layer comprises a material selected from the group consisting of methyl ester of acrylic acid, ethyl ester of acrylic acid, butyl ester of acrylic acid and 2-ethylhexyl ester of acrylic acid

37. The device of claim 33 wherein said pixel electrode comprises an indium tin oxide. –

REMARKS

The Examiner's Official Action dated July 21, 1999 has been received and its contents carefully noted. Filed concurrently herewith is a *Request for a One Month Extension of Time* which extends the shortened statutory period for response to November 21, 1999. Accordingly, applicant respectfully submits that this response is being timely filed.

Claims 1-8 and 11-16 were pending in the present application prior to the above amendment. Claims 4, 5, 7, 11, 15 and 16 have been have been amended and new claims 17-37 have been added to recite additional protection to which applicant is entitled. Accordingly, claims 1-8 and 11-37 are now pending in the present application and, for the reasons set forth in detail below, are believed to be in condition for allowance.